

## 10/11

[illegible]

Diagram illustrating a cross-sectional view of a semiconductor device structure. The structure shows three distinct gate regions defined by a common bottom layer (GL). The first gate region (left) consists of layers GI, GT, and GO. The second gate region (middle) consists of layers GI and CsT. The third gate region (right) consists of layers GO, GI, and SF. The layers are stacked on a common substrate (GL).

A detailed cross-sectional diagram of a semiconductor device. The structure is enclosed in a hatched frame. From left to right, it shows a series of horizontal layers and components. On the far left, a vertical section is labeled 'ART' and 'VT'. Moving right, there are three horizontal layers labeled 'AA', 'GT', and 'CsT'. Below these, there are three horizontal layers labeled 'GO', 'CP', and 'SL'. On the right side, there are three horizontal layers labeled 'GL' and 'SR'. The diagram uses various hatching patterns to distinguish different materials or regions.

A cross-sectional diagram of a semiconductor device. It shows a substrate with a trench structure. The trench is filled with a material labeled 'ESD'. The trench is lined with a material labeled 'CsT'. The trench is surrounded by a material labeled 'GO'. The trench is filled with a material labeled 'GI'. The trench is filled with a material labeled 'GT'. The trench is filled with a material labeled 'GO'. The trench is filled with a material labeled 'GI'. The trench is filled with a material labeled 'SF'. The trench is filled with a material labeled 'T'. The trench is filled with a material labeled 'GL'.